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Docket: TSMC 00 - 355  
S/N: 09/765,044

sfw AF/ 2823  
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To: Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

From: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject:

Serial No.: 09/765,044	Filed: 01/19/01
Inventor: Chyi-Tsong Ni	
Title: Method to Produce Porous Oxide	
Group Art Unit: 2823	Examiner: Brewster, W. M.
Attorney Docket: TSMC 00 - 355	

### APPEAL BRIEF

Dear Sir:

In response to the rejection of the claims in the above identified application for patent, made in the FINAL REJECTION in the office action, dated October 28, 2003, and the Advisory action dated January 30, 2004, Applicant filed a NOTICE OF APPEAL on March 1, 2004. Please accept our APPEAL BRIEF herewith together with the FEE of \$ 330. The commissioner is hereby authorized to charge payment of the above fee associated with this communication to Deposit account No. 19-0033. A duplicate copy of the request is enclosed. No oral hearing is requested.

Signature/Date

5/4/04

### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on

May 4, 2004

Signature/Date

5/4/04

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## APPEAL BRIEF

### 1. Real Party in Interest

The real party in interest is the assignee:

Taiwan Semiconductor Manufacturing Company  
No. 121 Park Avenue Rd. 3  
Science Based Industrial Park  
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this patent Application.

### 2. Related Appeals and Interferences

There are no related Appeals or Interferences.

### 3. Status of Claims:

Claims 1 to 34 are finally rejected under 35 U.S.C. § 103(a). No claims have been allowed.

### 4. Status of Amendments

On January 2, 2004, Applicants filed a Response to the Final Rejection dated 3/29/00. The Response sought to overcome the rejection of claims. In an Advisory Action dated October 28, 2003, the rejections were maintained. Claims 1 to 34 stand finally rejected. Claims 1 to 28 are as filed with claims 29 to 34 having been added during prosecution of the application.

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It is noted that layer numbered "22" in Fig. 3 as filed was amended to number -- 32 -- in substitute drawing sheet 1/1 with corresponding corrections

in the specification as filed at pages 9, 11 and 12 in the Response to the Office Action dated June 16, 2003.

5. Summary of the Invention

The invention provides a method of forming porous silicon oxide film by: pre-coating at least a portion of the inner walls of a CVD chamber with a layer of a first PECVD silicon oxide film having a first thermal CVD oxide deposition rate; placing a semiconductor wafer on the wafer chuck/heater within the pre-coated CVD chamber with the semiconductor wafer having an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate that is less than the first thermal CVD deposition rate of the first PECVD silicon oxide pre-coat film; and depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the inner walls of the CVD chamber.

CLAIM 1 (ORIGINAL) IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

1. (ORIGINAL) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8) providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the

CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18; PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls; and

d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7 AND 8; AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls.

CLAIM 11 (ORIGINAL) IS READ ON THE SPECIFICATION  
AND DRAWINGS AS FOLLOWS:

11. (ORIGINAL) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8)  
providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14;  
AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the  
CVD chamber inner walls with a layer of first PECVD silicon oxide film having a  
first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18;  
PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a  
semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber;  
the semiconductor wafer including an upper second PECVD silicon oxide film  
having a second thermal CVD oxide deposition rate thereupon that is less than the  
first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film  
coating the CVD chamber inner walls;

d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINE 19 TO PAGE  
9, LINE 2) pre-heating the semiconductor wafer; and

e) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7 AND 8;  
AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the  
upper second PECVD silicon oxide film overlying the semiconductor wafer by a  
thermal CVD process; the porous silicon oxide film being different from the first  
PECVD silicon oxide film coating the CVD chamber inner walls.

CLAIM 20 (ORIGINAL) IS READ ON THE SPECIFICATION  
AND DRAWINGS AS FOLLOWS:

20. (ORIGINAL) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8) providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18; PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINE 19 TO PAGE 9, LINE 2) pre-heating the semiconductor wafer; and

e) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7, 8, 16 AND 17; AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process temperature of from about 300 to 500°C; the porous silicon

oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls.

CLAIM 32 (PREVIOUSLY PRESENTED) IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

32. (PREVIOUSLY PRESENTED) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8) providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18; PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls; and



d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7, 8, 16 AND 17; AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

CLAIM 33 (PREVIOUSLY PRESENTED) IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

33. (PREVIOUSLY PRESENTED) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8) providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18; PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film

having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINE 19 TO PAGE 9, LINE 2) pre-heating the semiconductor wafer; and

e) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7, 8, 16 AND 17; AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

CLAIM 34 (PREVIOUSLY PRESENTED) IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

34. (PREVIOUSLY PRESENTED) A method for forming porous silicon oxide film, comprising the steps of:

a) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 6 TO 8) providing a CVD chamber having inner walls and a wafer chuck/heater;

b) (AS SEEN IN FIG. 1 AND SPECIFICATION PAGE 7, LINES 8 TO 14; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

c) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINES 17 AND 18; PAGE 9, LINES 3 AND 4; AND PAGE 11, LINE 15 TO PAGE 12, LINE 2) placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

d) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 8, LINE 19 TO PAGE 9, LINE 2) pre-heating the semiconductor wafer; and

e) (AS SEEN IN FIG. 2 AND SPECIFICATION PAGE 9, LINES 7, 8, 16 AND 17; AND PAGE 11, LINES 9 TO 14) depositing a porous silicon oxide film upon the

upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process temperature of from about 300 to 500°C; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

## 6. Issues

I. Whether or not claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 are patentable under 35 U.S.C. § 103(a) over Perng (U.S. Patent No. 6,149,987) in view of Ngo et al. (U.S. Patent No. 6,054,735).

II. Whether or not claims 3 to 7, 12 to 16, 21 to 25 and 32 to 34 are patentable under 35 U.S.C. § 103 (a) over Perng (U.S. Patent No. 6,149,987) in view of Ngo et al. (U.S. Patent No. 6,054,735) as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 above, and further in view of Tao (U.S. Patent No. 5,904,566).

## 7. Grouping of Claims

The rejected claims have been grouped together in the rejection as shown above in the issue. The claims do not all stand or fall together. Appellants urge that claims 1 to 34 are separately patentable. These claims are separately patentable for the reasons set forth in more detail below.

## 8. ARGUMENTS

### I. Applicant asserts that claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 are patentable under 35 U.S.C. § 103(a) over Perng (U.S. Patent No. 6,149,987) in View of Ngo et al. (U.S. Patent No. 6,054,735)

Reconsideration of the rejection of claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 under 35 U.S.C. § 103(a) as being unpatentable over Perng (U.S. Patent No. 6,149,987) (the '987 Perng Patent) in view of Ngo et al. (U.S. Patent No. 6,054,735) (the '735 Ngo Patent) is respectfully requested in view of the following remarks.

### II. Applicant asserts that claims 3 to 7, 12 to 16, 21 to 25 and 32 to 34 are patentable under 35 U.S.C. § 103(a) over Perng (U.S. Patent No. 6,149,987) in view of Ngo et al. (U.S. Patent No. 6,054,735) as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 above, and further in view of Tao (U.S. Patent No. 5,904,566)

Reconsideration of the rejection of claims 3 to 7, 12 to 16, 21 to 25 and 32 to 34 under 35 U.S.C. § 103(a) as being unpatentable over Perng (U.S. Patent No. 6,149,987) (the '987 Perng Patent) in view of Ngo et al. (U.S. Patent No. 6,054,735) (the '735 Ngo Patent) as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 above, and further in view of Tao (U.S. Patent No. 5,904,566) (the '566 Tao Patent) is respectfully requested in view of the following remarks.

Applicants have consolidated their arguments for efficiency and ease of understanding.

Applicants have previously amended Fig. 3 of the drawings to clarify that reference number "22" now only in Fig. 2, with film "22" in Fig. 3 now changed to -- 32-- are in reference to "the thermal CVD reactant gases will be

attracted, as at 22 of Fig. 2, towards pre-coated inner walls 14 more than towards the surface of wafer 18 having upper film 32."

Applicants' wish to briefly point up the claimed features of their invention which are believed to be not shown nor obvious from the teachings of known references in this field. The claims all clearly define:

- (1) pre-coating the inner walls of a CVD chamber with a first PECVD silicon oxide film having a first thermal CVD oxide deposition rate;
- (2) placing a semiconductor wafer within the pre-coated CVD chamber, the wafer having an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate that is less than the first thermal CVD oxide deposition rate of the first PECVD silicon oxide film coating the inner walls of the CVD chamber; and
- (3) depositing a porous silicon oxide film upon the semiconductor wafer's second PECVD silicon oxide film, the porous silicon oxide film being different from the first PECVD silicon oxide film coating the inner walls of the CVD chamber and such that the porous silicon oxide film is deposited upon the PECVD silicon oxide film coating the inner walls of the CVD chamber at a faster rate than upon the semiconductor wafer's second PECVD silicon oxide film.

Applicants urge that the '735 Ngo Patent teaches away from the claimed instant invention as it discloses seasoning a chamber with a film material and then depositing the *same* film material on a wafer. While, arguendo, "Ngo gives motivation in col. 1, lines 31-33, which facilitates producing a high quality uniform and very thin PECVD oxide layer" (Continuation Sheet to the 04/01/2003 Advisory Action. lines 17 and 18), such limitations are not claimed in the pending independent claims 1, 11, 20, 32, 33 and 34 in the instant application. Independent claim 1, for example, instead claims, inter alia, depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor

wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls.” (emphasis added)

Applicants respectfully disagree with what the Examiner states the '987 Perng Patent teaches at Col. 10, lines 5 to 25. Perng discloses at this instance that *instead* of reducing or eliminating surface sensitivity “to improve the film quality and rate of deposition of the SACVD layer” (Col. 10, lines 9 to 11), Perng “*enhances* surface sensitivity...”. (emphasis added) Col. 10, lines 19 and 20.

Again, the '987 Perng Patent not only does not disclose a pre-coating step, for which the Examiner cites Ngo, the combination does not disclose or teach that the:

(1) second thermal CVD oxide deposition rate (*referring to the subsequently formed porous silicon oxide film*) upon the upper second PECVD silicon oxide film on the semiconductor wafer is less than the

(2) first thermal CVD oxide deposition rate (*referring to the subsequently formed porous silicon oxide film*) upon the first PECVD silicon oxide film on the CVD chamber walls.

Applicants have italicized and bolded sections of the above argument to emphasize one of the key patentable differences between the claimed instant invention and Perng. Again, the wording "layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate" and the "upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate" from for example, Claim 1, lines 3 and 4 and lines 7 and 8, respectively, clearly define a second layer of PECVD silicon oxide film upon which *another layer* is deposited by a thermal CVD oxide process at a deposition rate that is less than the deposition rate of the *other layer* being deposited upon the first layer of PECVD

silicon oxide film. None of the references cited by the Examiner, alone or in combination, disclose or teach such limitations.

To further differentiate over the cited combination, the porous silicon oxide film 20 deposited upon the semiconductor wafer's 18 second PECVD silicon oxide film 22 is different from the first PECVD silicon oxide film 16 pre-coated upon the inner walls 14 of the CVD chamber 10.

Applicants further disagree with the Examiner's remarks at the first full paragraph of page 4 of the instant Office Action in that "As the two oxides [referring to Ngo first PECVD oxide formed with  $\text{SiH}_4$  and the second PECVD film with  $\text{O}_3$  and TEOS] are formed differently as claimed by the application, they would also display the feature of the porous oxide film depositing faster on the first PECVD than the second PECVD." Applicants' invention was rejected on the basis of 35 U.S.C. §103(a) and thus the references, Ngo, e.g., must show possession of the knowledge relied upon in the 103 combination however Ngo provides no such teaching. Applicants are not aware of anywhere in the applied references they any of them had possession of this limitation claimed in the instant invention. Thus, one skilled in the art would have no motivation to combine these references in a manner suggested by the Examiner.

Thus, independent claims 1, 11, 20, 32, 33 and 34 distinguish over: (1) the '987 Perng Patent in view of the '735 Ngo Patent under §103(a); and (2) the '987 Perng Patent in view of the '735 Ngo Patent as applied to claims 1, 2, 8 to 11, 17 to 20, 26 to 31 and 32 to 34 above and further in view of the '566 Tao Patent under §103(a); for the above reasoning and further because: Applicants urge that in fact there is an absence of "some teaching, suggestion or incentive supporting the prior art combination that produces the claimed invention;" (In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990); the prior art lack a suggestion that the reference should



be modified in a manner required to meet the claims; the invention is contrary to the teaching of the Ngo Patent—that is, the invention goes against the grain of what the prior art teaches; the Examiner has made a strained interpretation of the references that could be made only by hindsight; the Examiner has not presented a convincing line of reasoning as to why the claimed subject matter as a whole, including its differences over the prior art, would have been obvious; and the prior art references do not contain any suggestions (express or implied) that they be combined, or that they be combined in the manner suggested; the references take different approaches.

Claims 2 to 10 and 29 depend from independent claim 1; claims 12 to 19 and 30 depend from independent claim 11; claims 21 to 28 and 31 depend from independent claim 20; and are believed to distinguish over the combination for the reasons previously cited.

Therefore claims 1 to 34 are submitted to be allowable over the cited references and reconsideration and allowance are respectfully solicited.

#### **The Claims do not stand or fall together**

Claims 1 to 34 do not stand or fall together. The claims are separately and individually patentable.

Claims 2 to 10 and 29 depend from Parent Claim 1; claims 12 to 19 and 30 depend from Parent Claim 11; claims 21 to 28 and 31 depend from Parent Claim 20; Parent Claim 32 has no dependant claims; Parent Claim 33 has no dependant claims; and Parent Claim 34 has no dependant claims. Respective dependent Claims 2 to 10 and 29; 12 to 19 and 30; and 21 to 28 and 31, have non-obvious limitations that improve upon the invention's method of forming porous

silicon oxide film and are therefore separately patentable. Also, see above argument that explain in detail why the claims are non-obvious.

Specifically:

- a) the claim 2 limitation of including the step of pre-heating the semiconductor wafer before depositing the porous silicon oxide film is a non-obvious limitation not shown or taught by Perng nor Ngo in combination with the limitations of independent claim 1;
- b) the claim 3, 12 and 21 limitations of wherein the first PECVD silicon oxide film coating the CVD chamber inner walls has a thickness of from about 100 to 8000Å; the upper second PECVD silicon oxide film overlying the semiconductor wafer has a thickness of from about 100 to 2000Å; and the porous silicon oxide film has a thickness of preferably from about 500 to 10,000Å are non-obvious limitations not shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claims 1, 11 and 20;
- c) the claim 4 and 13 limitations of wherein the deposition of porous silicon oxide film is conducted at: a temperature from about 300 to 500°C; a TEOS flow rate from about 100 to 600 sccm; an ozone flow rate from about 1000 to 7000 sccm; and a time from about 20 to 400 seconds are non-obvious limitations not shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claims 1 and 11;
- d) the claim 22 limitations of wherein the thermal CVD deposition of porous silicon oxide film is further conducted at: a TEOS flow rate from about 100 to 600 sccm; an ozone flow rate from about 1000 to 7000 sccm; and a time from about 20 to 400 seconds are non-obvious limitations not

shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claim 20;

- e) the claim 5, 14 and 23 limitations of wherein the deposition of porous silicon oxide film is conducted at: a temperature from about 350 to 450°C; a TEOS flow rate from about 150 to 350 sccm; an ozone flow rate from about 4000 to 6000 sccm; and a time from about 50 to 350 seconds are non-obvious limitations not shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claims 1, 11 and 20;
- f) the claim 6, 15 and 24 limitation of wherein the deposited porous silicon oxide film has a density of from about 2.0 to 2.9 g/cm<sup>3</sup> is a non-obvious limitation not shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claims 1, 11 and 20;
- g) the claim 7, 16 and 25 limitation of wherein the deposited porous silicon oxide film has a density of from about 2.2 to 2.4 g/cm<sup>3</sup> is a non-obvious limitation not shown or taught by Perng nor Ngo in combination as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 nor further in view of Tao with the limitations of respective independent claims 1, 11 and 20;
- h) the claim 8, 17 and 26 limitations of wherein the first PECVD silicon oxide film pre-coating the CVD chamber inner walls is comprised of PE TEOS oxide; and the upper second PECVD silicon oxide film over the semiconductor wafer is comprised of PE SiH<sub>4</sub> oxide are non-obvious limitations not shown or taught by Perng nor Ngo in combination with the limitations of independent claims 1, 11 and 20;
- i) the claim 9, 18 and 27 limitation of including the step of pre-heating the semiconductor wafer to from about 250 to 500°C before depositing the

porous silicon oxide film is a non-obvious limitation not shown or taught by Perng nor Ngo in combination with the limitations of independent claims 1, 11 and 20;

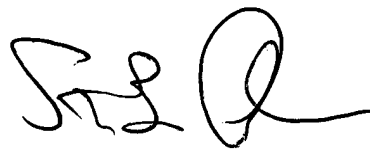
- j) the claim 10, 19 and 28 limitation of including the step of pre-heating the semiconductor wafer to from about 350 to 420°C before depositing the porous silicon oxide film is a non-obvious limitation not shown or taught by Perng nor Ngo in combination with the limitations of independent claims 1, 11 and 20; and
- k) the claim 29, 30 and 31 limitation of wherein the porous silicon oxide film is thermally deposited without plasma power is a non-obvious limitation not shown or taught by Perng nor Ngo in combination with the limitations of independent claims 1, 11 and 20.

Also, see the above argument that explain in detail why the claims are non-obvious over the cited combination of references.

CONCLUSION

Applicant requests that the Board of Appeals reverse the holding of the Examiner in finally rejecting Claims to 34 in the application. Allowance of all claims is requested.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'SBA', is written above a horizontal line.

Stephen B. Ackerman

Reg. No. 37,761

APPENDIX  
COPY OF THE CLAIMS

1. (original) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of  
5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is  
10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner  
15 walls.

2. (original) The method of claim 1, including the step of pre-heating the semiconductor wafer before depositing the porous silicon oxide film.

3. (original) The method of claim 1, wherein the first PECVD silicon oxide film coating the CVD chamber inner walls has a thickness of from about 100 to 8000Å; the upper second PECVD silicon oxide film overlying the semiconductor wafer has a thickness of from about 100 to 2000Å; and the porous silicon oxide film has a thickness of preferably from about 500 to 10,000Å.

4. (original) The method of claim 1, wherein the deposition of porous silicon oxide film is conducted at: a temperature from about 300 to 500°C; a TEOS flow rate from about 100 to 600 sccm; an ozone flow rate from about 1000 to 7000 sccm; and a time from about 20 to 400 seconds.

5. (original) The method of claim 1, wherein the deposition of porous silicon oxide film is conducted at: a temperature from about 350 to 450°C; a TEOS flow rate from about 150 to 350 sccm; an ozone flow rate from about 4000 to 6000 sccm; and a time from about 50 to 350 seconds.

6. (original) The method of claim 1, wherein the deposited porous silicon oxide film has a density of from about 2.0 to 2.9 g/cm<sup>3</sup>.

7. (original) The method of claim 1, wherein the deposited porous silicon oxide film has a density of from about 2.2 to 2.4 g/cm<sup>3</sup>.

8. (original) The method of claim 1, wherein the first PECVD silicon oxide film pre-coating the CVD chamber inner walls is comprised of PE TEOS oxide; and the upper second PECVD silicon oxide film over the semiconductor wafer is comprised of PE SiH<sub>4</sub> oxide.

9. (original) The method of claim 1, including the step of pre-heating the semiconductor wafer to from about 250 to 500°C before depositing the porous silicon oxide film.

10. (original) The method of claim 1, including the step of pre-heating the semiconductor wafer to from about 350 to 420°C before depositing the porous silicon oxide film.

11. (original) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of

5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is



10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process; the  
15 porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls.

12. (original) The method of claim 11, wherein the first PECVD silicon oxide film coating the CVD chamber inner walls has a thickness of from about 100 to 8000Å; the upper second PECVD silicon oxide film overlying the semiconductor wafer has a thickness of from about 100 to 2000Å; and the porous silicon oxide film has a thickness of from about 500 to 10,000Å.

13. (original) The method of claim 11, wherein the thermal CVD deposition of porous silicon oxide film is conducted at: a temperature from about 300 to 500°C; a TEOS flow rate from about 100 to 600 sccm; an ozone flow rate from about 1000 to 7000 sccm; and a time from about 20 to 400 seconds.

14. (original) The method of claim 11, wherein the thermal CVD deposition of porous silicon oxide film is conducted at: a temperature from about 350 to 450°C; a

TEOS flow rate from about 150 to 350 sccm; an ozone flow rate from about 4000 to 6000 sccm; and a time from about 50 to 350 seconds.

15. (original) The method of claim 11, wherein the thermal CVD deposited porous silicon oxide film has a density of from about 2.0 to 2.9 g/cm<sup>3</sup>.

16. (original) The method of claim 11, wherein the thermal CVD deposited porous silicon oxide film has a density of from about 2.2 to 2.4 g/cm<sup>3</sup>.

17. (original) The method of claim 11, wherein the first PECVD silicon oxide film pre-coating the CVD chamber inner walls is comprised of PE TEOS oxide; and the upper second PECVD silicon oxide film over the semiconductor wafer is comprised of PE SiH<sub>4</sub> oxide.

18. (original) The method of claim 11, wherein the semiconductor wafer is pre-heated to from about 250 to 500°C.

19. (original) The method of claim 11, wherein the semiconductor wafer is pre-heated from about 350 to 420°C.

20. (original) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of

5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is  
10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process  
15 temperature of from about 300 to 500°C; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls.

21. (original) The method of claim 20, wherein the first PECVD silicon oxide film coating the CVD chamber inner walls has a thickness of from about 100 to 8000Å; the upper second PECVD silicon oxide film overlying the semiconductor wafer has a thickness of from about 100 to 2000Å; and the porous silicon oxide film has a thickness of from about 500 to 10,000Å.

22. (original) The method of claim 20, wherein the thermal CVD deposition of porous silicon oxide film is further conducted at: a TEOS flow rate from about 100 to 600 sccm; an ozone flow rate from about 1000 to 7000 sccm; and a time from about 20 to 400 seconds.

23. (original) The method of claim 20, wherein the thermal CVD deposition of porous silicon oxide film is conducted at: a temperature from about 350 to 450°C; a TEOS flow rate from about 150 to 350 sccm; an ozone flow rate from about 4000 to 6000 sccm; and a time from about 50 to 350 seconds.

24. (original) The method of claim 20, wherein the thermal CVD deposited porous silicon oxide film has a density of from about 2.0 to 2.9 g/cm<sup>3</sup>.

25. (original) The method of claim 20, wherein the thermal CVD deposited porous silicon oxide film has a density of from about 2.2 to 2.4 g/cm<sup>3</sup>.

26. (original) The method of claim 20, wherein the first PECVD silicon oxide film pre-coating the CVD chamber inner walls is comprised of PE TEOS oxide; and the upper second PECVD silicon oxide film over the semiconductor wafer is comprised of PE SiH<sub>4</sub> oxide.

27. (original) The method of claim 20, wherein the semiconductor wafer is pre-heated to from about 250 to 500°C.

28. (previously presented) The method of claim 20, wherein the semiconductor wafer is pre-heated from about 350 to 420°C.

29. (previously presented) The method of claim 1, wherein the porous silicon oxide film is thermally deposited without plasma power.

30. (previously presented) The method of claim 11, wherein the porous silicon oxide film is thermally deposited without plasma power.

31. (previously presented) The method of claim 20, wherein the porous silicon oxide film is thermally deposited without plasma power.

32. (previously presented) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of

5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is  
10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner  
15 walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

33. (previously presented) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;  
pre-coating at least a portion of the CVD chamber inner walls with a layer of  
5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is  
10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process; the  
15 porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

34. (previously presented) A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of  
5 first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is  
10 less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process

- 15 temperature of from about 300 to 500°C; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.